REMARKS

The Office Action dated February 2, 2003 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. In view of the following remarks, Applicants request the favorable consideration of claims 1-12.

The Office Action rejected claims 1, 2, and 4-12 under 35 U.S.C. § 103(a) over Usami (U.S. Patent No. 6,205,516B1) in view of Fadavi-Ardekani (U.S. Patent No. 6,401,176). The Office Action took the position that the combination of the cited references teach or suggest all the features recited in claims 1, 2, and 4-12. Applicants respectfully disagree.

Claim 1 recites a synchronous DRAM comprising, one memory array divided into a plurality of memory blocks, mode storage units so disposed in a plurality of stages as to correspond to the memory blocks, for storing control information for defining operation modes of the memory blocks. A setting unit is provided for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. A mode selection unit is provided for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted, and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of the memory blocks in accordance with the control information stored in the mode storage unit selected.

The essence of the claimed invention is a single SDRAM comprising multiple mode storage units, a setting unit, a mode selection unit and an access unit. The claimed

invention provides the advantage of performing independent operation in different operation modes in one SDRAM. Thus, the claimed invention provides the benefit of allowing memory blocks to independently operate in an operation mode represented by the control information stored in the corresponding mode storage unit. As a result, a plurality of controllers requiring different operation modes can share the single SDRAM. Thus, it is respectfully submitted that the applied references fail to disclose or suggest the features of Applicants' invention, and therefore fails to provide the advantages which are provided by the present invention.

Usami discloses a method for designating a unique address data to select mode operations via mode register 35. More specifically, Usami discloses a memory control circuit 5a that is utilized to control the ROM 2, the internal RAM 3, and the extended RAM 4. The internal RAM 3 is constructed from 8 SDRAMS. However, Usami does not teach or suggest a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. In other words, Usami only discloses a control circuit that is contained in an external ASIC for setting the mode registers in various SDRAMS. Thus, Usami neither teaches nor suggests the feature of changing the operation modes in one SDRAM as recited in the claimed invention. Thus, Usami fails to teach or suggest a synchronous DRAM comprising a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. In addition, as admitted in the Office Action, Usami

fails to teach that the programmable registers are programmed via instructions outputted from a plurality of controllers.

Fadavi-Ardekani discloses the shared usage of a synchronous memory by a plurality of agents or processors. However, Fadavi-Ardekani does not cure the deficiencies of Usami. In particular, Fadavi-Ardenkani neither teaches nor suggests a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. In addition, the applied reference does not teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by the address inputted. Thus, Fadavi-Ardekani does not cure the deficiencies of Usami. As a result, Applicants respectfully submit that applied references neither teach nor suggest the features recited in claim 1. Therefore, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2, and 4-12 are dependent upon independent claim 1. Therefore, claims 2, and 4-12, for at least the reasons mentioned above, recite subject matter that is neither taught nor suggested by the applied references. Applicants respectfully request the withdrawal of the rejection of claims 2 and 4-12 under 35 U.S.C. 103(a).

The Office Action rejected claims 1-12 under 35 U.S.C. § 103(a) over Rao (U.S. Patent No. 6,173,356B1) in view of Usami. The Office Action takes the position that the combination of Rao and Usami teach or suggest all the features recited in claims 1-12. Applicants respectfully disagree.

Rao discloses a multiprocessor that includes a memory system having a memory

controller for linking a plurality of processors with an integrated memory. Rao further discloses mode registers 415 that are used for setting optional access modes such as page reads and writes or burst access with a selected burst type. See Column 11 Lines 2-4. Rao, however, does not teach or suggest a setting unit for setting the control information designated by a mode setting instructions to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instructions outputted from a plurality of controllers. Rao also does not teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted. In other words, Rao does not disclose a method for changing the operation modes of a SDRAM.

As discussed above, Usami fails to teach or suggest a synchronous DRAM comprising a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. Furthermore, Usami fails to teach or suggest the deficiencies of Rao. Thus, the combination of Rao and Usami fail to teach or suggest a synchronous DRAM comprising a setting unit, a mode selection unit, and an access unit as recited in the Claimed invention. As a result, Applicants respectfully submit that claim 1 recites subject matter this patentable. Therefore, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2-12 depend upon independent claim 1, therefore it is submitted that these claims, for at least the reasons mentioned above, likewise recite subject matter that is

neither taught nor suggested by the applied references. As a result, Applicants request the withdrawal of the rejection of claims 2-12 under 35 U.S.C. 103(a).

Claims 1-10 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Farrer (U.S. Patent 5, 307, 320) in view of Fadavi-Ardekani (U.S. Patent 6,401,176). The Office Action the position that the combination of Farrer and Fadavi-Ardekani disclose all the features recited in claims 1-10 and 12. Applicants respectfully disagree.

Farrer is directed to a memory controller for a dynamic random access memory. The memory controller includes multiple programmable storage registers, where one register is associated with every bank location in the memory array. More specifically, Farrer discloses that each programmable register is independently programmed to contain access parameters that are necessary to access its associated bank. Thus, Farrer merely discloses a memory controller that can be adaptive to various types of DRAM banks by associating programmable storage registers with each DRAM bank. Farrer as stated by the Office Action fails to disclose a synchronous DRAM or that the programmable registers are programmed via instructions outputted from a plurality of controllers.

The Office Action takes the position that Fadavi-Ardekani discloses the deficiencies of Farrer. Applicants respectfully disagree.

As mentioned above, Fadavi-Ardekani discloses the shared usage of a synchronous memory by a plurality of agents or processors. However, Fadavi-Ardekani fails to cure the deficiencies of Farrer. In particular, the applied reference fail to teach or suggest a synchronous DRAM comprising a setting unit, a mode selection unit, and an access unit as recited in the claimed invention. More specifically, the applied references do not teach or suggest an SDRAM having multiple mode registers so as to perform the independent

operations in different operation modes in the single SDRAM. In other words, applied references either alone or in combination fail to teach or suggest a synchronous DRAM having a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. The applied references also fail to teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted, and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of the memory blocks in accordance with the control information stored in the mode storage unit selected. Thus, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2-10, and 12 depend upon independent claim 1, therefore it is submitted that these claims, for at least the reasons mentioned above, likewise recite subject matter that is neither taught nor suggested by the applied references. As a result, Applicants request the withdrawal of the rejection of claims 2-10, and 12 under 35 U.S.C. 103(a).

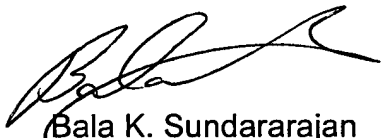
In view of the above remarks, Applicants respectfully request the withdrawal of the rejection of claims 1-12. Applicants submit that claims 1-12 recite subject matter this is neither taught nor suggested by the applied references. Accordingly, Applicants request the favorable consideration and prompt allowance of claims 1-12.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100021-00046.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



Bala K. Sundararajan
Attorney for Applicants
Reg. No. 50,900

Customer No. 004372
1050 Connecticut Ave. NW
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6261
Fax: (202) 638-4810

BKS:bgk

Enclosures: Petition for Extension of Time